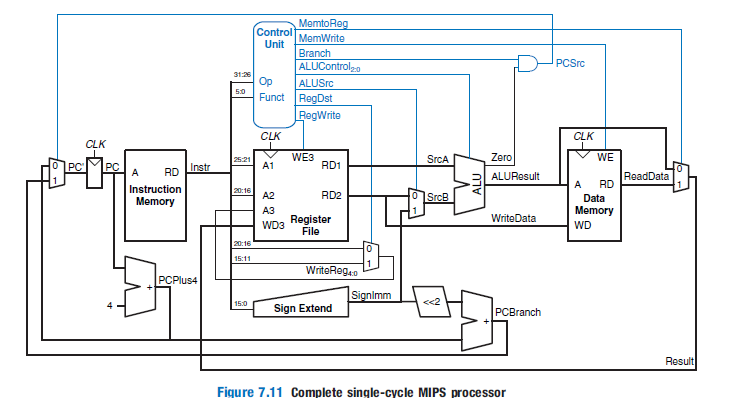
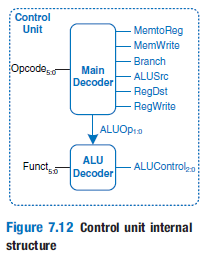
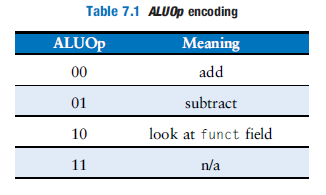
**MIPS Single cycle processor**

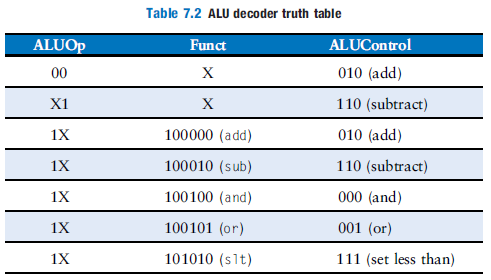
Design correction: J instruction support – mux not included before PC register (look in the book 7.33)



**ALU OPs:**



**ALU Truth Table:**



**Main Decoder Truth Table:**

